



Parallel-Processing Equalizers for Multi-Gbps Communications

One can compromise among computational efficiency, complexity of circuitry, and processing rates.

NASA's Jet Propulsion Laboratory, Pasadena, California

Architectures have been proposed for the design of frequency-domain least-mean-square complex equalizers that would be integral parts of parallel-processing digital receivers of multigigahertz radio signals and other quadrature-phase-shift-keying (QPSK) or 16-quadrature-amplitude-modulation (16-QAM) of data signals at rates of multiple gigabits per second. "Equalizers" as used here denotes receiver subsystems that compensate for distortions in the phase and frequency responses of the broad-band radio-frequency channels typically used to convey such signals. The proposed architectures are suitable for realization in very-large-scale integrated (VLSI) circuitry and, in particular, complementary metal oxide semiconductor (CMOS) application-specific integrated circuits (ASICs) operating at frequencies lower than modulation symbol rates.

A digital receiver of the type to which the proposed architecture applies (see Figure 1) would include an analog-to-digital converter (A/D) operating at a rate, f_s , of 4 samples per symbol period. To obtain the high speed necessary for sampling, the A/D and a 1:16 demultiplexer immediately following it would be constructed as GaAs integrated circuits. The parallel-processing circuitry downstream of the demultiplexer, including a demodulator followed by an equalizer, would operate at a rate of only $f_s/16$ (in other words, at 1/4 of the symbol rate). The output from the equalizer would be four parallel streams of in-phase (I) and quadrature (Q) samples.

The proposed architectures would implement subconvolution (see Figure 2), fast-Fourier-transform/inverse-fast-Fourier-transform (FFT-IDFT), and discrete-Fourier-transform/inverse-discrete-Fourier-transform (DFT-IDFT) overlap-and-save filter algorithms. A key property of the proposed architectures is that one can make engineering compromises among computational efficiency, complexity of circuitry, and processing rates. Such trades are made

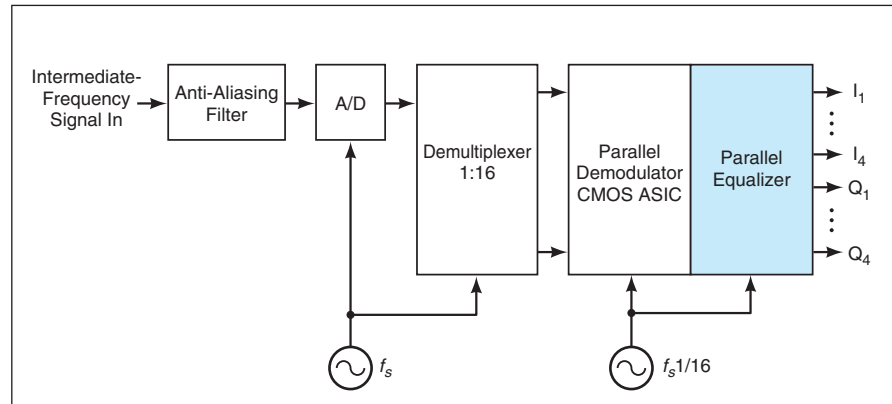


Figure 1. A Parallel-Processing Digital Receiver would include a parallel-processing equalizer.

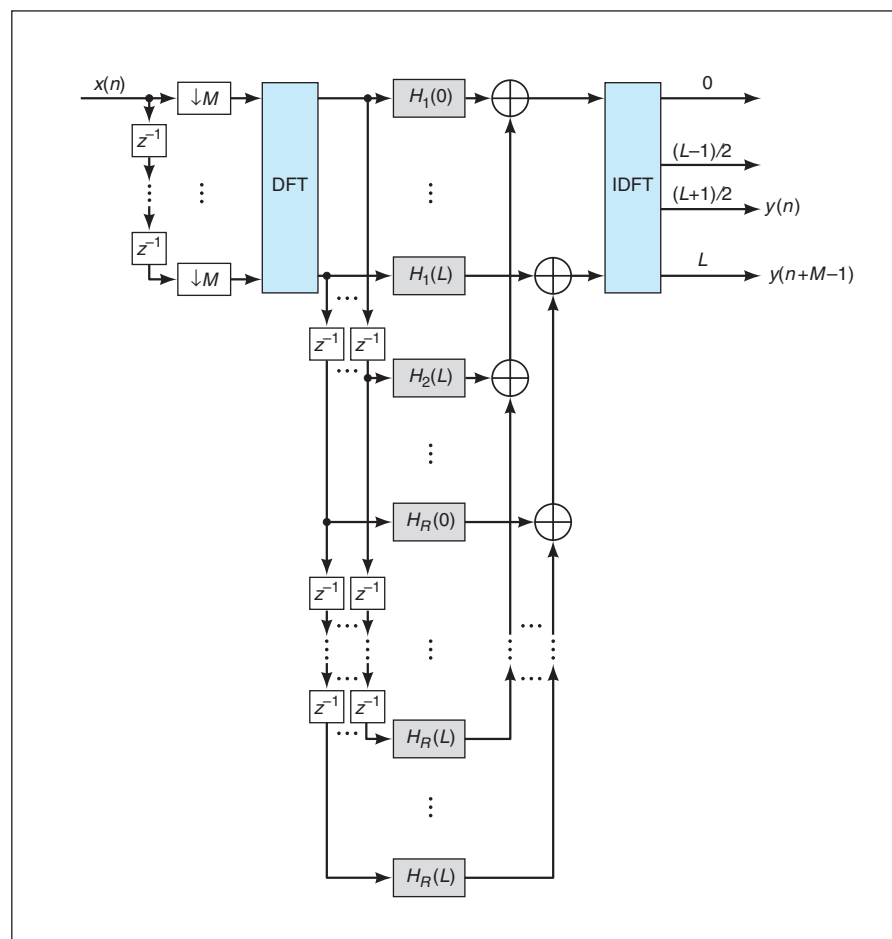


Figure 2. A Parallel Subconvolution Filter Bank would perform R subconvolutions, each of length $L+1$, at $1/M$ of the input sample rate. The symbol z^{-1} denotes a delay of one sample period, " $\downarrow 16$ " signifies decimation by a factor of 16, and H_i denotes a frequency-domain digital filter.

possible, in part, by utilizing subconvolutions and relatively simple digital signal-processing methods in such a manner as to eliminate a lower bound imposed on FFT-IFFT lengths by equalizer tap lengths. For a given receiver, the equalizer tap length would theoretically be unlimited, and the FFT-IFFT length could be chosen completely independently of the equalizer tap length. The FFT-IFFT length could be determined on the basis of the de-

sired reduction in the processing rate. The specific values chosen for the proposed architectures are an equalizer tap length of 32, with an FFT-IFFT length of 8 chosen to enable processing at 1/4 of the symbol rate.

This work was done by Andrew Gray, Parminder Ghuman, Scott Hoy, and Edgar H. Satorius of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

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AlN-Based Packaging for SiC High-Temperature Electronics **Electronic packaging can withstand a continuous temperature of 500 °C.**

John H. Glenn Research Center, Cleveland, Ohio

Packaging made primarily of aluminum nitride has been developed to enclose silicon carbide-based integrated circuits (ICs), including circuits containing SiC-based power diodes, that are capable of operation under conditions more severe than can be withstood by silicon-based integrated circuits. A major objective of this development was to enable packaged SiC electronic circuits to operate continuously at temperatures up to 500 °C. AlN-packaged SiC electronic circuits have commercial potential for incorporation into high-power electronic equipment and into sensors that must withstand high temperatures and/or high pressures in diverse applications that include exploration in outer space, well logging, and monitoring of nuclear power systems. This packaging embodies concepts drawn from flip-chip packaging of silicon-based integrated circuits. One or more SiC-based circuit chips are mounted on an aluminum nitride package substrate or sandwiched between two such substrates. Intimate electrical

connections between metal conductors on the chip(s) and the metal conductors on external circuits are made by direct bonding to interconnections on the package substrate(s) and/or by use of holes through the package substrate(s). This approach eliminates the need for wire bonds, which have been the most vulnerable links in conventional electronic circuitry in hostile environments. Moreover, the elimination of wire bonds makes it possible to pack chips more densely than was previously possible.

Especially notable components of packaging of this type are the following:

- AlN substrates that have high thermal conductivity [170 W/(m·K)] and a coefficient of thermal expansion (CTE) that matches that of SiC;
- Thick gold conductor film circuit traces, the adhesion and sheet resistance of which do not change measurably at 500 °C over time periods as long as 1,000 hours; and
- Glass passivation/sealing layers that have a breakdown potential of 2,575 V

at room temperature and, at 500 °C, breakdown potentials of 1,100 V for encapsulation of Au conductors and 1,585 V for encapsulation of Pt conductors.

The matching of CTEs minimizes thermal stresses. Packaging interconnections are monometallic or bimetallic and able to withstand high temperatures. These and other features are known to contribute to reliability at high temperatures and are expected to extend the high-temperature functionality of the packaged electronic devices. Further research will be necessary to characterize the long-term reliability of SiC-based circuits in AlN-based packages.

This work was done by Ender Savrun of Sienna Technologies, Inc., for Glenn Research Center. For further information, access <http://www.siennatech.com>.

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